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Comparative analysis of Dual Tail Comparator using Clock Gating Technique

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Abstract: **This paper presents the comparison of dynamic latch comparator with dual tail comparator. Dual input in the circuit is compared and single output respective to the input provided is acquired from the opposite end. Comparator circuit should consume less power and should have a high speed of operation. With the proposed design the amenities of the comparator circuit is obtained. Since scaling of transistor size is taking place, so the circuit is designed in 45nm technology. The supply voltage for the circuit is also very low as compared to other conventional based design. With the proposed design the efficiency of the circuit obtained is higher than the conventional design with reduction in the leakage current and leakage power in the design. The circuit is simulated at 45 nm technology with the supply voltage of 0.7 volts.**

Keywords: **dynamic latch comparator, dual tail comparator, power consumption, speed, efficiency, leakage power**

I. INTRODUCTION

Comparator circuit is the basic building block of both digital and analog circuit. Circuit is used for the comparison of both the voltage and current signal. Basically two or more than two inputs are provided in the comparator circuit and single output is obtained from the other end depending of the input signal provided to it. Various designs where comparator circuit is used are in analog to digital signal, for sampling of the data, for comparison of voltage and current signals etc. Op-amp based design is used earlier for the designing of the comparator circuit. Differential pair circuit is the basic comparator design. With the advancement in the VLSI technology scaling of the transistor sizing is taking place. So the circuit is designed with cmos transistor, FinFET for the better and effective result of the circuit. Clocked comparator circuit consists of 3 phases: pre-amplification, decision circuit and post-amplification circuit as shown in Fig1.

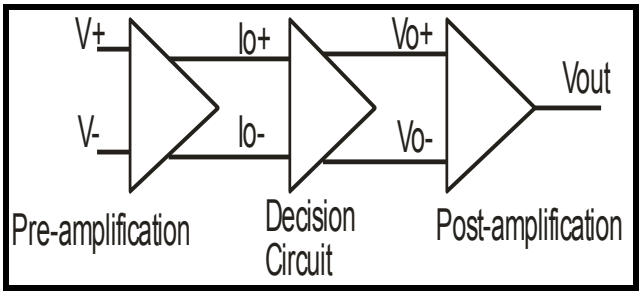

Fig1. Block Diagram of Comparator

Modifications in the circuit are being done for designing a good and effective circuit. Using the truth table of the basic comparator circuit one bit comparator circuit is designed and further eight bit comparator circuit is designed afterwards. It is observed that with the decreased in the current in the circuit power dissipation in the circuit is also decreasing effectively [1]. Variable Switching Voltage (VSV) circuit is implied in the flash ADC circuit for increasing the speed of operation in the design with lowering the peak power consumption in the design. The circuit is simulated in 65nm technology. A higher linearity is obtained using it with faster response time [2]. Comparator circuit is designed using the regenerative

latch and SR latch. With the inclusion of the latch in the circuit the kickback noise in the circuit is reduced. Circuit is operated with low voltage and with higher speed. With the elimination of the kickback noise faster speed in the design is obtained [3]. ADC circuit with preamplifier and regenerative latch provides with faster operation speed and better sensitivity in the design. Input referred offset voltage is also adjusted using the proposed design of the circuit [4]. Circuit is designed using two differential circuits. Differential circuits replacing the normal input leads to faster output response with lower power consumption in the design. A better response in terms of speed and power consumption is obtained using it [5].

Comparator circuit is used for various applications in the design. Comparator circuit is used with back-gate and clock boosting technique. These designs are used in low voltage and wide range operation. It is used in small signal processing and basically in SOC [6]. Differential signal is placed in place of normal input of the comparator circuit. With the proposed design a higher operating speed with lower power consumption in the circuit is obtained [7]. Dual tail circuit came into existence for the higher output response in the circuit. The circuit is designed for operating with higher speed and lower power consumption [8]. Circuit is modified with triple-tail cell. The main advantage of the circuit as compared to other design is the operation of circuit at higher speed. It has better output response as compared to the conventional design [9]. For further reducing the power consumption and leakage power in the design clock gating technique is used. Clock gating technique is applied in the dual tail circuit for the reduction of power consumption in the design along with faster speed of operation [10]-[11]. Dual tail comparator circuit is compared with the conventional comparator design and the output of the circuit is observed and calculated. A better and effective result is acquired using the former design [12]. Clock gating technique is implemented in the dual tail circuit. The modified circuit shows faster operating speed with lower power consumption in the design [13]. Dual tail comparator circuit is simulated in cadence and parameters of the circuit is observed and calculated. Various conventional circuits are simulated along with the proposed design. Comparison of all the circuit is observed and made with the proposed design [14].

II. WORKING OF DYNAMIC LATCH COMPARATOR CIRCUIT

Conventional dynamic latch comparator circuit has high input impedance, rail-to-rail output swing and lower static power consumption. The operation of the circuit works in two phases: Firstly the reset phase. It includes when the clock "clk" = 0 and Mtail is off. During this phase the transistor M7 and M8 will get reset. Thus it will pull both the output i.e., outp and outn to VDD and thus it then is the starting condition of the circuit or the circuit is in reset phase. The cmos implementation of dynamic latch comparator is shown in Fig2. Second is the comparison phase i.e., when the "clk" = VDD. Transistor M7 and M8 will be off and Mtail will be on. Both the output outp and outn are on VDD. They eventually start to get discharged at different rates. When Vinp>Vinn then outp discharges at a much faster rate than outn, and hence outp discharged by drain current of transistor M2, falls down to VDD before outn which is being discharged by drain current of transistor M1. Thus the PMOS transistor M5 will get turn on leading to latch regenerative speed. This causes back-to-back regenerative feedback path by transistor M3, M5, M4 and M6. Thus outp discharges to ground and outn pulls to VDD. When Vinp<Vinn the reverse process follows.

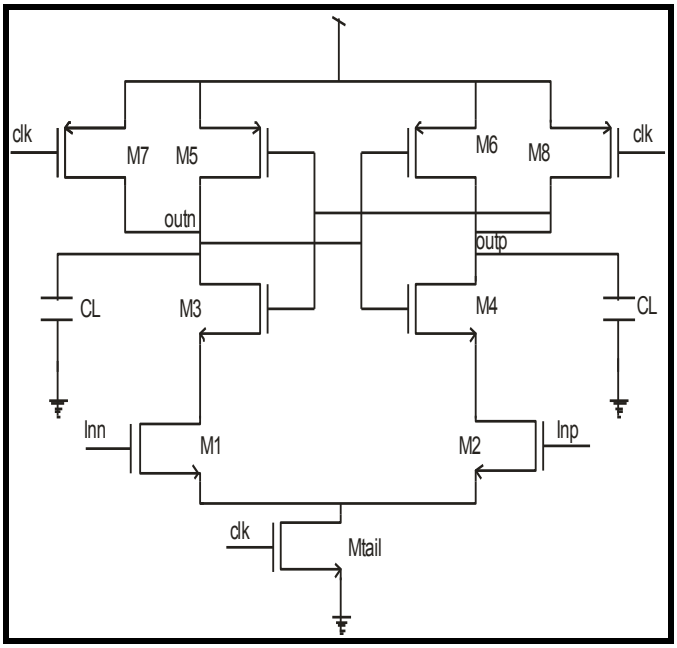

Fig2. Dynamic Latch Comparator

III. WORKING OF DYNAMIC LATCH COMPARATOR USING CLOCK GATING

Clock gating phenomenon is used in the circuit for controlling the clock signal given in the circuit. As we know clock dissipates nearly 70% of power in the circuit, so clock gating in the circuit is done. Clock gating is basically of two types: Local gating and Global gating. In the former one gating signal is provided to separate module in the circuit while in the later one gating is provided to the universal clock pulse which further is distributed to the entire circuit in the design. Clock gating implementation is depicted in Fig3.

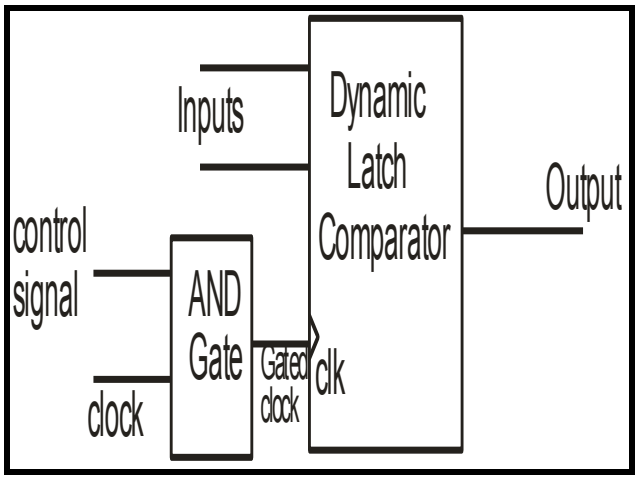

Fig3. Dynamic Latch Comparator using Clock Gating

In the circuit when both the enable signal and clock signal is high then the gated signal will proceed further and the output from the circuit will be obtained.

IV. WORKING OF DUAL TAIL COMPARATOR CIRCUIT

The main advantage of the circuit from the other conventional design is operating at lower supply voltage. Dual tail circuit enables large current in latching stage along with wider Mtail2 in the regenerative latching path. It is independent of input common mode voltage with small current in input stage for low offset. In the reset phase clk = 0, Mtail1 and Mtail2 are off. M3 and M4 transistor are pre-charged, fn and fp nodes to V_{DD} which further causes transistors MR1 and MR2 causing the output nodes to ground signal. During the decision making phase i.e., clk = V_{DD} , Mtail1 and Mtail2 is on. This leads to transistors M3 and M4 turning off which further leads to voltage drop from nodes fn and fp. Transistors MR1 and MR2 forms the intermediate stage. Node fn passes from the cross coupled inverter and result in good shielding between the input and output signal leading to reduction of kickback noise. CMOS implementation of dual tail comparator circuit is depicted in Fig4.

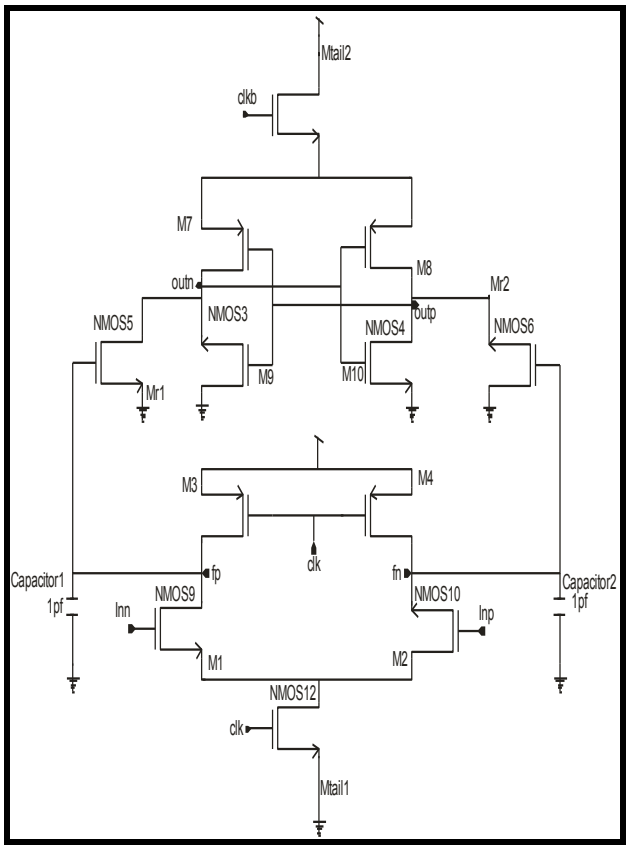

Fig4. Dual Tail Comparator Circuit

The output voltage acquired at the first stage output at time t0 has its effect on the initial differential output voltage with latch delay. Delay of the circuit is reduced by the design. In the intermediate stage, transistor will be in cutoff mode fn and fp nodes are discharged to ground. During the reset phase, the nodes are charged from ground to V_{DD} causing high transient noise in the regeneration time with low kickback noise voltage.

The circuit has higher energy with input referred as offset voltage than conventional dynamic latch comparator. The dual tail circuit consists of two current paths which further increases the performance of the circuit.

V. PARAMETERS CALCULATED

1) Power Consumption
2) Delay
3) Power-delay Product
4) Voltage Gain
5) Efficiency
6) Leakage Power

POWER CONSUMPTION

It is defined as the total power consumed by the circuit. Power consumption in the circuit means how much power

should be provided in order to drive a load and provide us output. Power consumption causes due to two factors: static and dynamic. Static power comes into existence when circuit is in idle mode. It is defined as the product of voltage and current. While dynamic power is defined as the power consumption in the run mode. It is proportional to the switching activity of the clock pulse, capacitance, supply voltage and frequency of the design. More the supply voltage, more the power consumption in the circuit.

$$\text{Power (Ptotal)} = \text{Static power} + \text{Dynamic Power} \quad (1)$$

$$P(t) = (Vdd) * (Idd(t)) \quad (2)$$
$$P(\text{dynamic}) = \alpha C (Vdd)^2 f \quad (3)$$
$$P(\text{static}) = I(\text{static}) * Vdd \quad (4)$$

Energy consumed by the circuit is given by

$$E = \int_0^T (Vdd)\big(Idd(t)\big)\, dt \quad (5)$$

$$Pavg = \frac{E}{T} = \left(\frac{1}{T}\right) \int_0^T (Vdd)\big(Idd(t)\big)\, dt \quad (6)$$

Table I. Comparison table of Power Consumption

	Dynamic Latch Comparator	Clock Gating in Dynamic Latch Comparator	Dual Tail Comparator Circuit
Watt	13.07n	64.39p	740.0f

DELAY

The most important property of a comparator circuit is the operating speed of the circuit. Delay in circuit is defined as the time taken to provide us with output when input is provided to the circuit. It occurs due to the presence of parasitic capacitance in the design. The charging and discharging of parasitic capacitance causes the occurrence of propagation delay in the circuit. Using the dual tail technique the operating speed of the circuit is higher as compared to the conventional design of comparator.

$$\text{Delay } (\tau) = 0.69\ RC \quad (7)$$
$$\text{Delay } (\tau) = \frac{T(rf) + T(fr)}{2} \quad (8)$$

Where T (rf) = time for rising to falling and T (fr) = time for falling to rising

Table II. Comparison table of Propagation Delay

	Dynamic Latch Comparator	Clock Gating in Dynamic Latch	Dual Tail Comparator Circuit
		Comparator	
nsec	12.609	10.56	9.32

Fig5. represents the comparison chart of delay of the circuits.

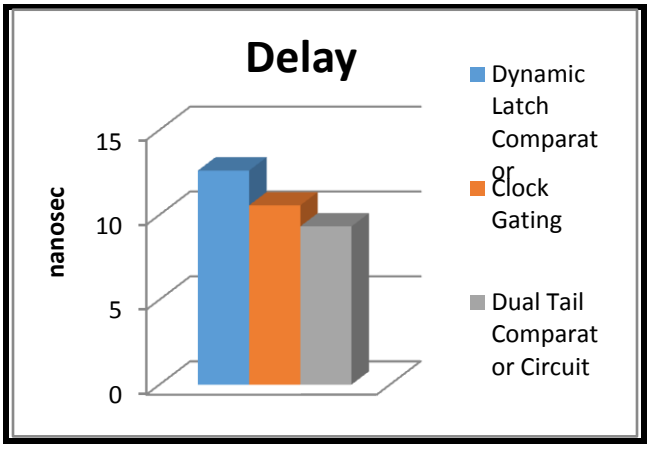

Fig5. Comparison Chart of Delay

POWER-DELAY PRODUCT

It is defined as the product of both the power consumption and propagation delay of the circuit. Lower the power delay product of the circuit, better the circuit is.

$$PDP = Pavg * (\tau) \quad (9)$$

Table III. Comparison table of Power–Delay Product

	Dynamic Latch Comparator	Clock Gating in Dynamic Latch Comparator	Dual Tail Comparator Circuit
pdp	164.79e-18	6.79e-19	6.89e-21

VOLTAGE GAIN

It is defined as the ratio of output voltage to input voltage. Voltage gain is measured in terms of dB. With the dual tail technique in the circuit, voltage gain in the circuit has increased effectively.

$$Voltage\ Gain = 10 \log\left(\frac{Vout}{Vin}\right) dB \quad (10)$$

Vout is Output Voltage acquired and *Vin* is Input Voltage supplied

Table IV. Comparison table of Voltage Gain

	Dynamic	Clock	Dual Tail

	Latch Comparator	Gating in Dynamic Latch Comparator	Comparator Circuit
dB	18.09	20.40	21.4

Fig6. represents the comparison chart of voltage gain of the circuits.

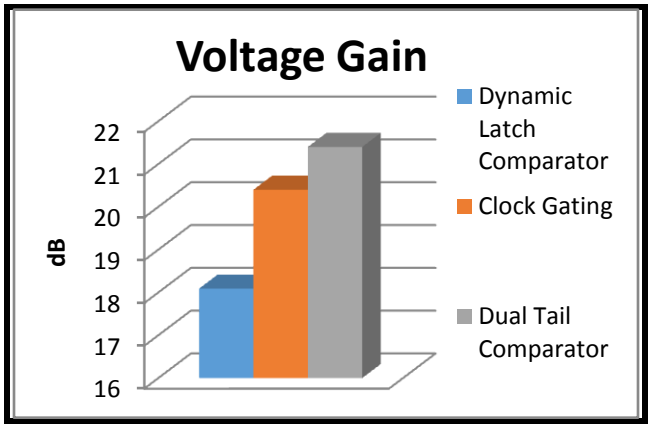

Fig6. Comparison Chart of Voltage Gain

EFFICIENCY

It is calculated as the ratio of both output power to input power. If is defined in terms of percentage. With the dual tail comparator circuit a better and efficient output for the circuit is acquired.

$$\eta = \frac{Pout}{Pin} \qquad (11)$$

Where, *Pout* is the power calculated at the output terminal and *Pin* is Power delivered at the input

Table V. Comparison table of Efficiency

	Dynamic Latch Comparator	Clock Gating in Dynamic Latch Comparator	Dual Tail Comparator Circuit
%	28.9	29.6	46.5

Fig7. represents the comparison chart of efficiency of the circuits.

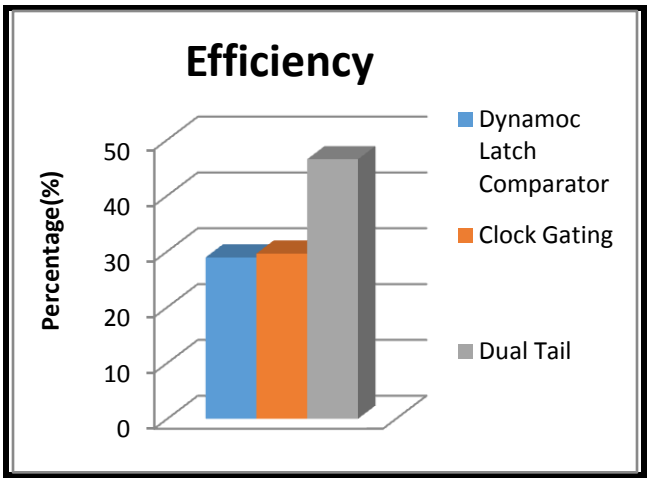

Fig7. Comparison Chart of Efficiency

LEAKAGE POWER

Due to the presence of short channel effects leakage power occurs in the transistor. It occurs basically when the circuit is sin sleep mode. Leakage current can lead to losing of data and thus leakage current along with leakage power should be minimal for the circuit. It is the product of leakage current and leakage power in the circuit.

$$P\ (leak) = I\ (leak) * Voltage \qquad (12)$$

Table VI. Comparison table of Leakage Power

	Dynamic Latch Comparator	Clock Gating in Dynamic Latch Comparator	Dual Tail Comparator Circuit
pW	100.6	72.31	26.84

Fig8. represents the comparison chart of efficiency of the circuits.

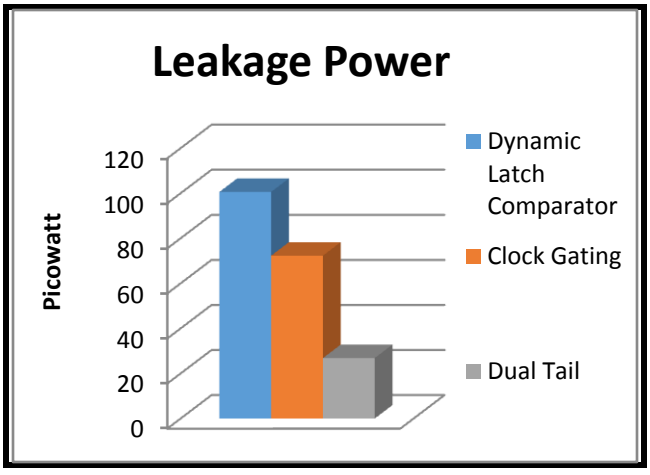

Fig8. Comparison Chart of Leakage Power

VI. OUTPUT WAVEFORMS OBTAINED

1. The output of the comparator circuit is shown in Fig9. Input and output of the circuit at time interval is shown in the figure.

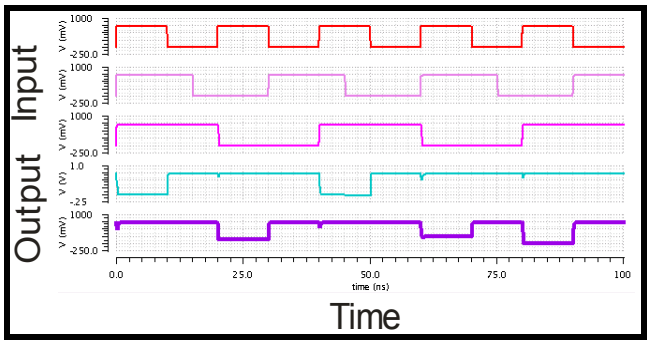

Fig9. Output of Comparator Circuit

2. Power consumption of the conventional comparator circuit is shown in Fig10.

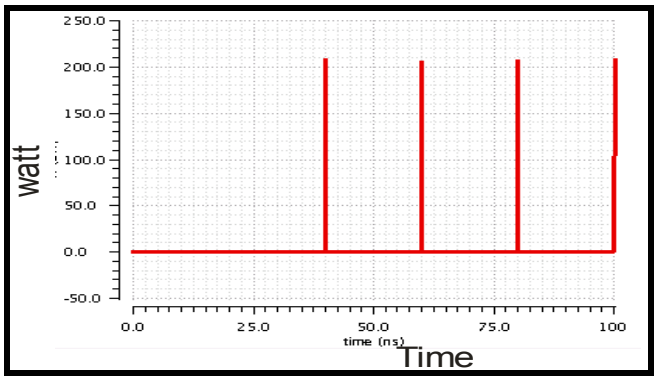

Fig10. Power Consumption Graph

3. Leakage Power of the conventional circuit is shown in Fig11.

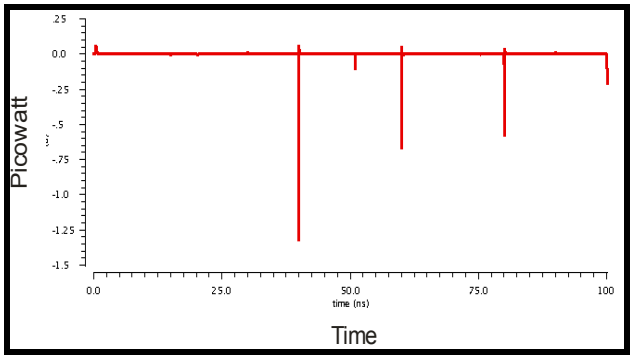

Fig11. Leakage Power Graph

VII. CONCLUSION

The comparison of three circuits is being done. All the circuits are simulated in 45nm technology with the supply voltage of 0.7 volt. Dual tail comparator circuit provides a higher voltage gain, efficiency with reducing the power consumption, propagation delay, leakage power in the design. The dual tail circuit provides with better and efficient output at a faster rate and with low supply voltage. Parameters like power consumption, power-delay product and leakage power is reduced by 98%, 98.9% and 73.32% respectively. While the voltage gain and efficiency in the circuit is raised by 18% and 60% respectively. With the proposed design the delay in the circuit is reduced to 9.32 nsec from 12.609 nsec respectively.

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